



FIG. 1

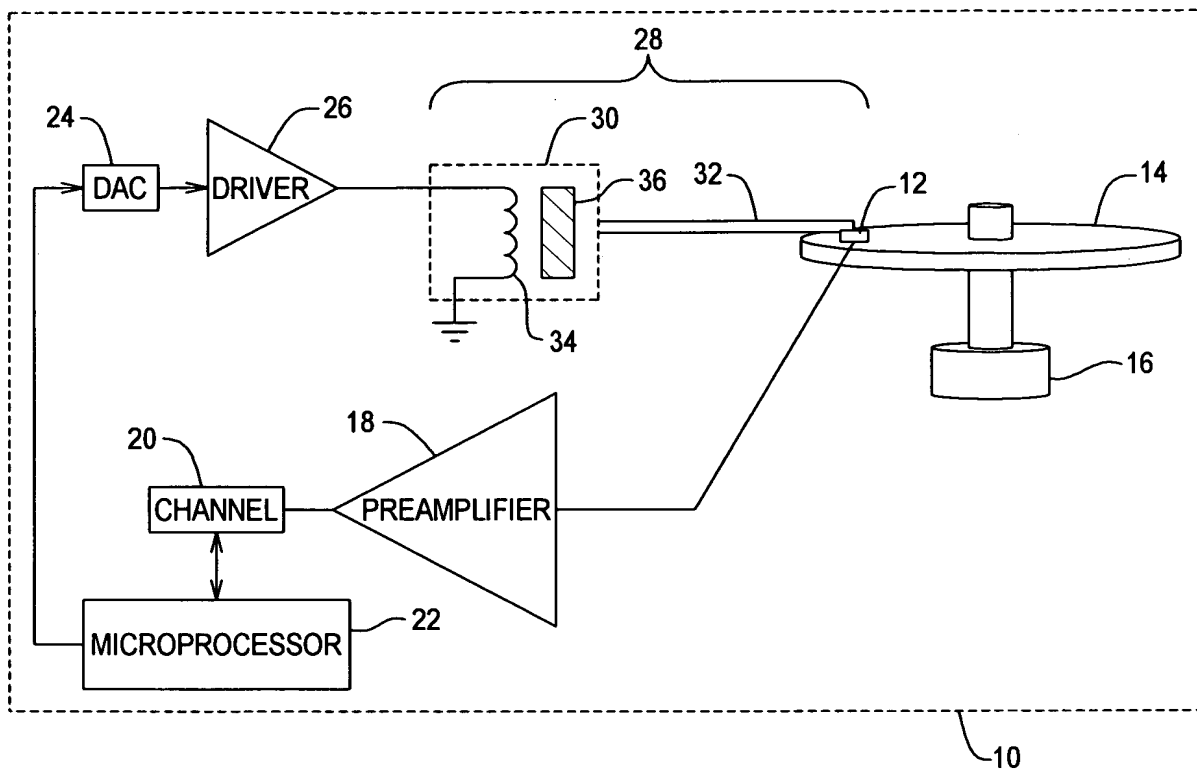


FIG. 2

The diagram illustrates the internal circuitry of a programmable logic device (PLD) 26. It features a VREF input, a VCC input, and a COMMAND CURRENT input. The circuit includes several voltage dividers (48, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90) and buffers (52, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90) to provide VREF and VCC signals to various internal blocks. A COMMAND CURRENT input is connected to a resistor (48) and a capacitor (46). The circuit is divided into several functional blocks, including a VREF divider (48, 46), a VREF buffer (52), a VREF divider (54), a VREF divider (56), a VREF divider (58), a VREF divider (60), a VREF divider (62), a VREF divider (64), a VREF divider (66), a VREF divider (68), a VREF divider (70), a VREF divider (72), a VREF divider (74), a VREF divider (76), a VREF divider (78), a VREF divider (80), a VREF divider (82), a VREF divider (84), a VREF divider (86), a VREF divider (88), a VREF divider (90).

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FIG. 4

